

FIG. 1 is a diagram of a prior art system for detecting data bits b_n from received signals r_n . The system includes an Equalizer (210), a 3 level slicer (220), and an MLT-3 decoder (250). The Equalizer (210) receives the received signals r_n and outputs a signal to the 3 level slicer (220). The 3 level slicer (220) outputs a signal to the MLT-3 decoder (250), which then outputs the detected data bits b_n .

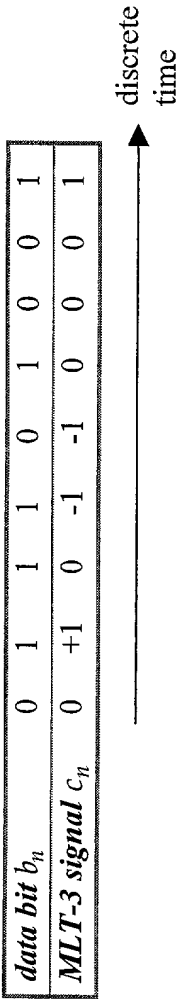


FIG. 1
PRIOR ART

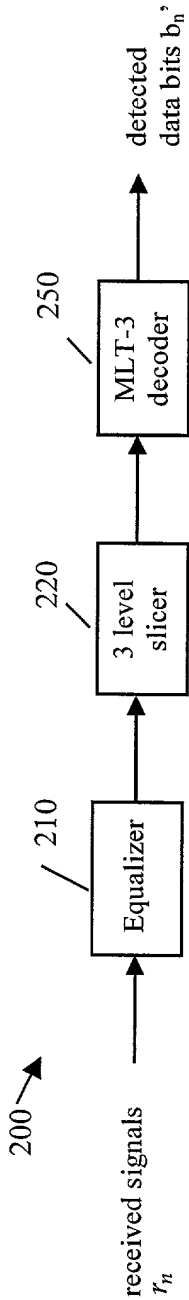


FIG. 2
PRIOR ART

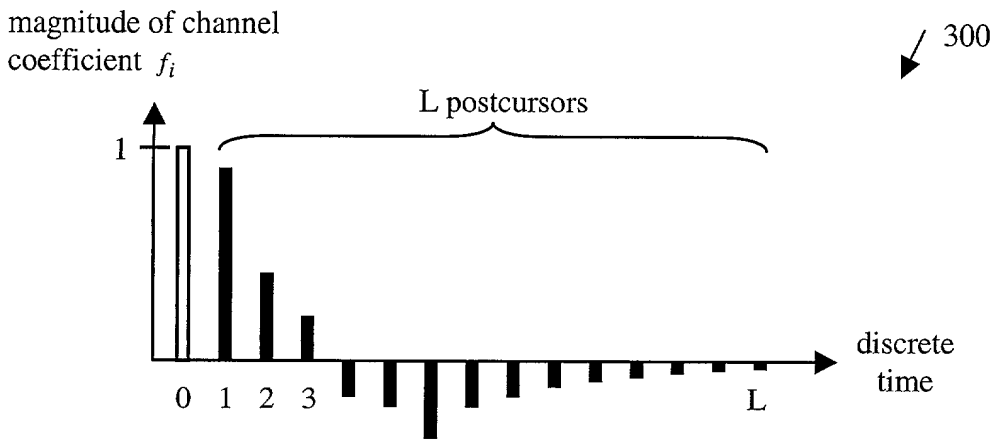


FIG. 3
PRIOR ART

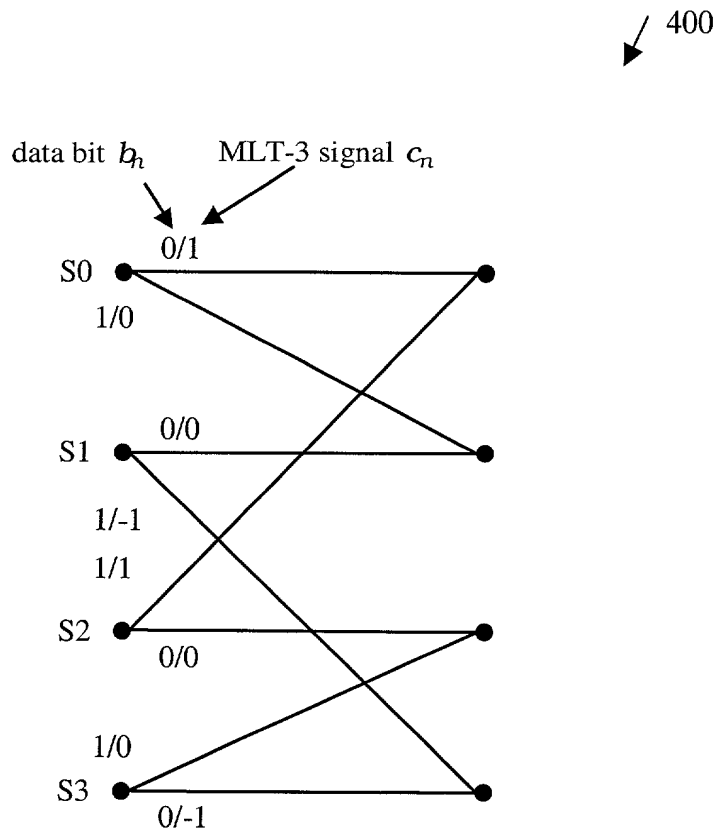


FIG. 4

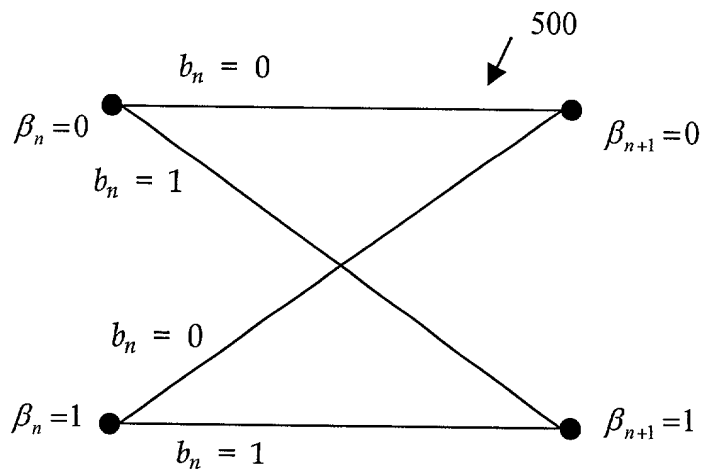


FIG. 5

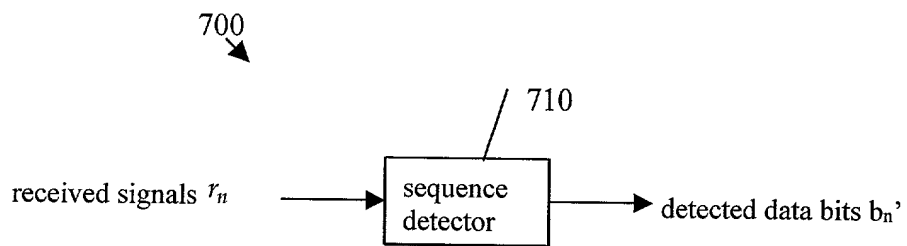


FIG. 7

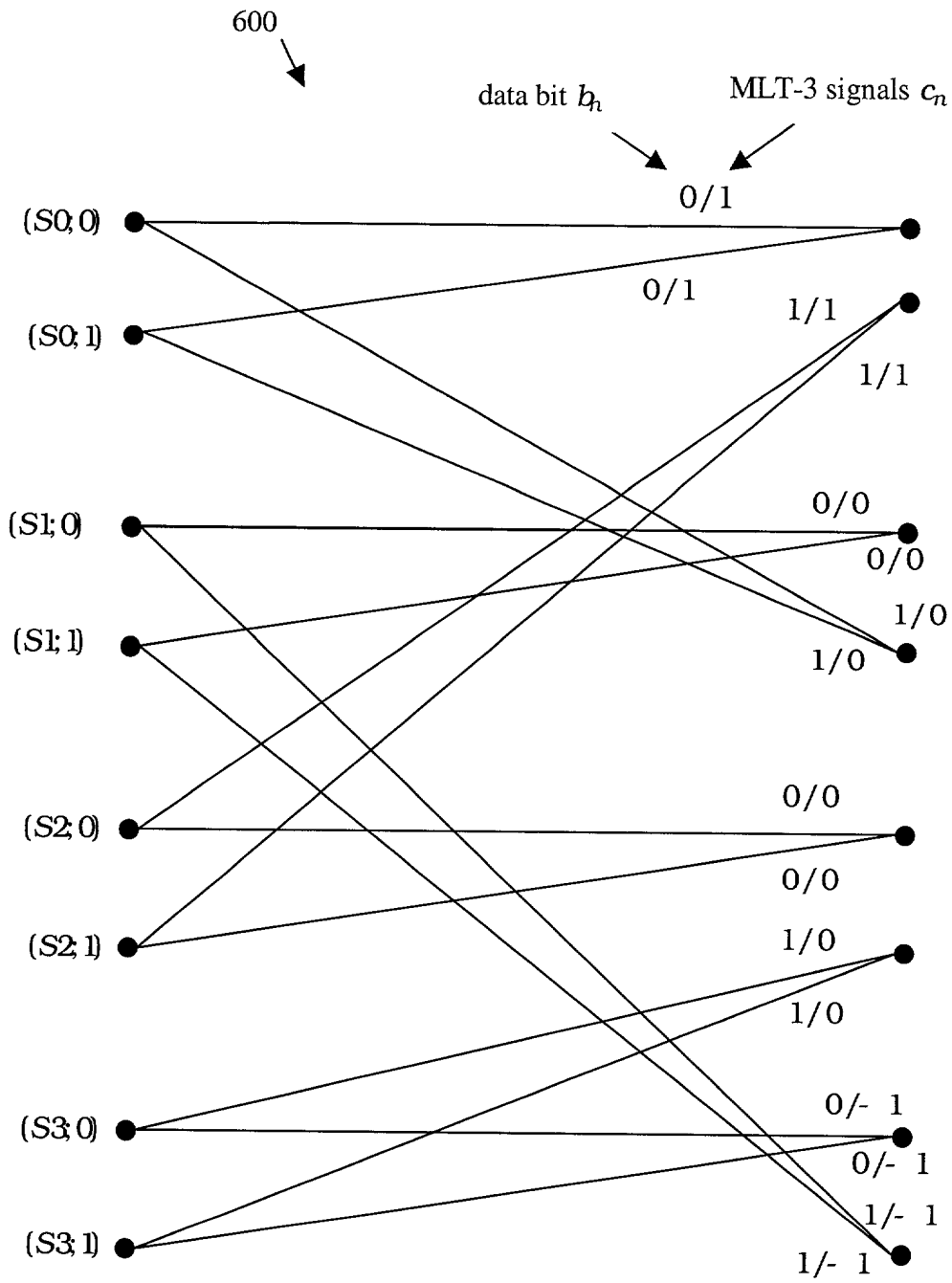


FIG. 6

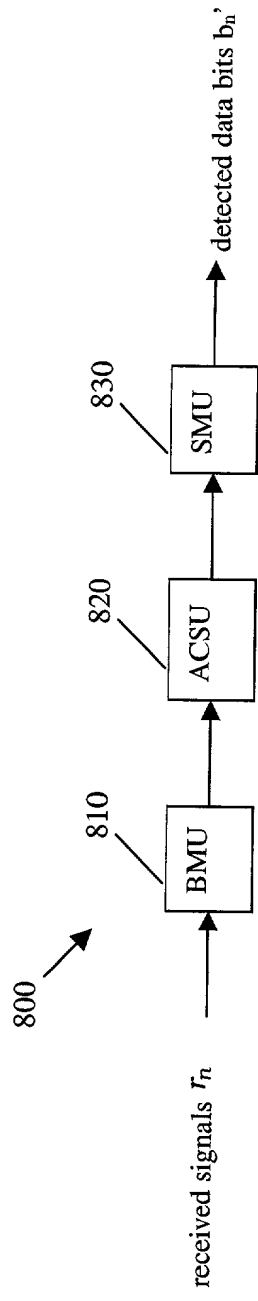


FIG. 8

900

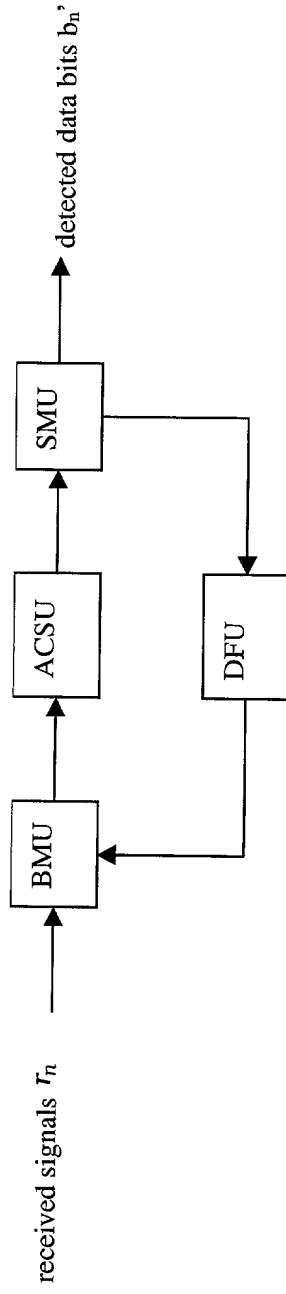


FIG. 9